# Axel Feldmann

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EDUCATION	<b>Massachusetts Institute of Technology</b> , Cambridge, Massachusetts Ph.D. in Electrical Engineering and Computer Science	anticipated in December 2024
	<ul> <li>Advisor: Daniel Sanchez</li> <li>S.M. in Electrical Engineering and Computer Science</li> <li>GPA: 5.0 / 5.0</li> </ul>	May 2021
	<b>Carnegie Mellon University</b> , Pittsburgh, Pennsylvania BS in Computer Science • GPA: 3.9 / 4.0	May 2019

Selected coursework: computer architecture, operating systems, compilers, algorithms, computer networks, numerical algorithms

#### **EXPERIENCE Research Assistant**

MIT CSAIL - Cambridge, MA

- Currently working on designing hardware accelerators for sparse linear algebra, specifically focused on scientific computing.
- Designed *Spatula*, an accelerator for sparse matrix factorization that outperforms GPU baselines by 47×.
- Worked on designing hardware accelerators for Fully Homomorphic Encryption (FHE), a computationally expensive cryptographic system that enables arithmetic operations on encrypted data.
- Designed *F1*, the first proposed ASIC accelerator capable of executing entire FHE programs.
- Developed compilation techniques that enabled F1 and CraterLake (our second-generation accelerator design) to achieve  $5000 \times$  speedups over CPU baselines.

#### Intern

Cerebras Systems - Sunnyvale, CA

- Worked on the CSL (Cerebras Systems Language) team to designing new abstractions for programming the Cerebras Wafer Scale Engine.
- Designed and built a complete MPI-style collectives library for CSL programmers.

### **Undergraduate Research Assistant**

Computer Organization Research Group - Pittsburgh, PA

- Worked with Prof. Nathan Beckmann on *Livia*, a system architecture for data centric computing.
- Created zsim-based simulation infrastructure to evaluate our proposed architecture.
- Wrote applications to effectively utilize Livia's novel hardware features.

## **Systems Software Intern**

NVIDIA - Santa Clara, CA

- Improved display driver performance for existing and upcoming Tegra SoCs.
- Reduced kernel test time by 30% via improved thread synchronization.

#### **Software Engineering Intern**

Yahoo, Flurry Analytics - Sunnyvale, CA

- Created webapp to help users design metrics API queries.
- Re-engineering User Acquisition Analysis (UAA) features on the Flurry data platform.

PAPERS	Spatula: A Hardware Accelerator for Sparse Matrix Factorization
	Axel Feldmann, Daniel Sanchez, <i>MICRO 2023</i> .
	An Architecture to Accelerate Computation on Encrypted Data
	Axel Feldmann*, Nikola Samardzic*, Aleksander Krastev, Srinivas Devadas, Ronald Dreslinski, Chris
	Peikert, Daniel Sanchez, IEEE Micro Top Picks 2022.

CraterLake: A Hardware Accelerator for Efficient Unbounded Computation on Encrypted Data Nikola Samardzic, Axel Feldmann, Aleksander Krastev, Nathan Manohar, Nicholas Genise, Srinivas Devadas, Chris Peikert, Daniel Sanchez, ISCA 2022.

F1: A Fast and Programmable Accelerator for Fully Homomorphic Encryption Axel Feldmann\*, Nikola Samardzic\*, Aleksander Krastev, Srinivas Devadas, Ron Dreslinski, Chris Peikert, Daniel Sanchez, MICRO 2021.

Summer 2018

Summer 2017

September 2019 – present

Summer 2022

2018 - 2019

	Livia: Data-Centric Computing Throughout the Memory Hierarchy Eliot Lockerman, <b>Axel Feldmann</b> , Mohammad Bakhshalipour, Alexandru Stanescu, Shashw Daniel Sanchez, and Nathan Beckmann, <i>ASPLOS 2020</i> .	vat Gupta,	
TEACHING	<ul><li>15-410: Operating System Design and Implementation, CMU</li><li>Held office hours and designed class projects.</li><li>Graded student projects and exams.</li></ul>	2018-2019	
	Teaching Assistant215-213: Introduction to Computer Systems, CMU•• Taught a recitation section and held office hours.• Graded student projects and exams.	2017-2018	
SKILLS	Computer architecture research, hardware prototyping/development, parallel programming analytical and simulation-based performance modeling, hardware-software codesign. C++, C, Python, Rust, CUDA, x86/64 assembly, Julia, PyTorch, Triton, Pandas, cuBLAS, cuSP	and simulation-based performance modeling, hardware-software codesign.	

[Resume compiled on 2023-12-05]